

**IN THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

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1. (currently amended) A system comprising:  
an external non-dedicated synchronous memory including a plurality of memory banks;  
a first agent ~~having~~ providing a single first agent clock signal adapted to control access to a first ~~memory~~ portion of said non-dedicated synchronous memory including a first number of said plurality of memory banks;  
and  
a second agent ~~lacking a dedicated clock,~~ receiving said ~~memory access~~ first agent clock signal from said first agent, and providing ~~having~~ a second agent clock signal ~~representation of said first agent's clock signal~~ adapted to access a second ~~memory portion of said non-dedicated synchronous memory~~ including a second number of said plurality of memory banks;  
wherein said second agent clock signal is synchronized to and in-phase with said first agent clock signal; and  
said first number and said second number being variable.
2. (original) The system according to claim 1, further comprising:  
a register to set at least one of said first number and said second number.
3. (original) The system according to claim 1, wherein:  
said register is adapted to be set by either one of said first agent and said second agent.
4. (original) The system according to claim 1, wherein:  
a value set in said register is adapted to correspond to said first number of said plurality of memory banks.
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5. (original) The system according to claim 1, wherein:  
said second number is a remainder of said plurality of said memory banks after said first number of said plurality of memory banks.

6. (original) The system according to claim 1, wherein:  
said first agent is a first digital signal processor; and  
said second agent is a second digital signal processor.

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7. (currently amended) A system comprising:  
a plurality of agents;  
an external non-dedicated shared synchronous memory block accessible by each of said plurality of agents, said external non-dedicated shared memory block including a plurality of memory banks; and  
a register adapted to partition said external non-dedicated shared synchronous memory block into a plurality of partitions, each of said plurality of partitions being accessible by a unique group of said plurality of agents; and  
wherein said plurality of partitions each comprise a number of said plurality of memory banks; and  
wherein said plurality of agents, ~~lacking a dedicated clock signal,~~  
each receive a common base clock signal from another agent and access said external non-dedicated shared synchronous memory block with clock a memory access signal ~~representations of a synchronized and in phase with said common~~  
base clock signal.

8. (original) The system according to claim 7, wherein:  
said register is settable by at least one of said plurality of agents.

9. (canceled)

10. (canceled)

11. (canceled)

12. (currently amended) The system according to claim 8 40,  
wherein:

said non-dedicated shared synchronous memory is synchronous  
dynamic random access memory.

I/ 13. (currently amended) A system for providing access to shared  
external non-dedicated synchronous memory, said system comprising:

a first agent to provide a single first agent memory access clock  
signal to allow said first agent to access said shared external non-dedicated  
synchronous memory; and

a second agent ~~lacking a dedicated clock~~, receiving said single first  
agent memory access clock signal from said first agent, ~~to provide a~~  
~~representation of said single~~ and providing a second agent memory access clock  
signal to access said shared external non-dedicated synchronous memory in  
synchronism with said access by said first agent to said shared external non-  
dedicated synchronous memory;

wherein each of said first agent and said second agent may access  
different portions of said shared external non-dedicated memory simultaneously.

14. (currently amended) The system for providing access to shared  
external non-dedicated synchronous memory according to claim 13, wherein:

said shared external non-dedicated synchronous memory services  
in turn said first agent and said second agent without a wait state therebetween.

15. (currently amended) The system for providing access to shared external non-dedicated synchronous memory according to claim 13, wherein:

said shared external non-dedicated synchronous memory block is partitioned such that said first agent has access to a first partition of said shared external non-dedicated synchronous memory block [[:]] and said second agent has access to a second partition of said shared external non-dedicated synchronous memory block.

16. (currently amended) The system for providing access to shared external non-dedicated synchronous memory according to claim 13, wherein:

said first agent is a first digital signal processor; and  
said second agent is a second digital signal processor.

17. (currently amended) A method of synchronizing access from a plurality of agents to external non-dedicated shared synchronous memory, comprising:

providing a single memory access clock signal;

providing a representation of said single memory access clock signal in synchronism and in phase with said single memory access clock signal;

firstly accessing a portion of said external non-dedicated shared synchronous memory from a first agent based on said single memory access clock signal; and

secondly accessing a portion of said external non-dedicated shared synchronous memory from a second agent based on said representation of said single memory access clock signal ~~received from said first agent;~~

wherein said ~~step of~~ secondly accessing said ~~external non-dedicated shared memory~~ follows said ~~step of~~ firstly accessing without a wait state therebetween.

18. (currently amended) The method of synchronizing access from a plurality of agents to shared synchronous memory according to claim 17, ~~further comprising wherein:~~

~~regenerating in~~ said second agent generates said ~~single~~ representation of said memory access clock signal.

I, 19. (currently amended) The method of synchronizing access from a plurality of agents to shared synchronous memory according to claim 17, wherein:

said first agent provides said ~~single~~ memory access clock signal.

20. (currently amended) A method of partitioning an external non-dedicated shared synchronous memory, comprising:

setting a configuration register to partition said external non-dedicated shared synchronous memory into a first plurality of synchronous memory banks and a second plurality of synchronous memory banks;

accessing said first plurality of synchronous memory banks from a first agent;

accessing said second plurality of synchronous memory banks from a second agent; and

re-partitioning said external non-dedicated shared synchronous memory on-the-fly;

wherein said second agent ~~lacks a dedicated clock and~~ receives a clock signal ~~representation of from~~ said first agent's clock signal and generates a second agent clock signal for a said second agent's access to said non-dedicated shared synchronous memory.

21. (currently amended) The method of partitioning a an external non-dedicated shared synchronous memory according to claim 20, wherein:

said ~~step~~ of re-partitioning is performed from said first agent.

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22. (currently amended) Apparatus for synchronizing access from a plurality of agents to shared synchronous memory, said apparatus comprising:

- means for providing a ~~single~~ memory access clock signal;
- means for firstly accessing said shared synchronous memory from a first agent based on said ~~single~~ memory access clock signal;
- means for secondly accessing said shared synchronous memory from a second agent based on a second agent memory access clock signal synchronized and in-phase with said single memory access clock signal;

wherein said means for second accessing accesses said shared synchronous memory without a wait state after said means for firstly accessing said shared synchronous memory accesses said shared synchronous memory.

23. (currently amended) Apparatus for partitioning a shared synchronous memory, said apparatus comprising:

- means for setting a configuration register to partition said shared synchronous memory into a first plurality of synchronous memory banks and a second plurality of synchronous memory banks;
- means for accessing said first plurality of synchronous memory banks from a first agent;
- means for accessing said second plurality of synchronous memory banks from a second agent that receives a clock signal ~~representation of said from said first agent's clock signal and lacks a dedicated clock agent and generates a second agent clock signal in synchronism and in-phase with said received clock signal~~, for said second agent's access to said shared synchronous memory;
- means for re-partitioning said shared synchronous memory on-the-fly.